

**What is claimed is:**

1           1. A method for compensating non-linearity errors in A/D converter conversion  
2 operations associated with converting analog image data from a CMOS imager to  
3 digital data, comprising:

4           (a) isolating an A/D converter from the CMOS imager;

5           (b) applying a plurality of analog voltages to the isolated A/D converter, the  
6 plurality of voltages ranging from analog ground to a full-scale voltage level;

7           (c) measuring and storing a difference between an output from the isolated A/D  
8 converter and a reference value associated with the analog voltage being applied to the  
9 isolated A/D converter; and

10          (d) correcting the non-linearity of the isolated the isolated A/D converter using  
11 the stored difference.

1           2. The method as claimed in claim 1, wherein the plurality of applied analog  
2 voltages are analog ground, 0.25 of the full-scale voltage level, 0.5 of the full-scale  
3 voltage level, 0.75 of the full-scale voltage level, and the full-scale voltage level.

1           3. A circuit for compensating errors in correlated double sampling amplifiers  
2 and/or A/D converters associated with a CMOS imager having columns of pixels,  
3 comprising:

4           a reference voltage source to produce test voltages;

5           a test switch operatively connected between said reference voltage source and a  
6 correlated double sampling amplifier;

7           a test switch control line, operatively connected to said test switch, to apply a  
8   signal to said test switch, said signal controlling an ON/OFF state of said test switch,  
9   said test switch applying a test voltage from said reference voltage source to the  
10   correlated double sampling amplifier when the state of said test switch is ON; and  
11           a measurement circuit to measure a difference between an output of the A/D  
12   converter produced from a test voltage being applied to the correlated double sampling  
13   amplifier through said test switch and a reference voltage associated with the applied  
14   test voltage to determine an error in the correlated double sampling amplifier and/or  
15   A/D converter.

1           4. The circuit as claimed in claim 3, further comprising:

2           an isolation switch operatively connected between a column of pixels and an  
3   associated correlated double sampling amplifier to effectively electrically isolate the  
4   column of pixels from the associated correlated double sampling amplifier;

5           said isolation switch being in an OFF state when said test switch is in an ON  
6   state.

1           5. The circuit as claimed in claim 3, wherein said reference voltage source  
2   produces a voltage corresponding to a full-scale voltage level to enable said  
3   measurement circuit to determine a gain error in the correlated double sampling  
4   amplifier and/or A/D converter.

1           6. The circuit as claimed in claim 3, wherein said reference voltage source  
2   produces a voltage corresponding to ground to enable said measurement circuit to

3 determine an offset error in the correlated double sampling amplifier and/or A/D  
4 converter.

1       7. The circuit as claimed in claim 3, wherein said reference voltage source  
2 produces a sequence of two voltages with a difference corresponding to a full-scale  
3 voltage level minus a predetermined maximum anticipated variation voltage to enable  
4 said measurement circuit to determine a gain error in the correlated double sampling  
5 amplifier and/or A/D converter.

1       8. The circuit as claimed in claim 7, wherein said predetermined maximum  
2 anticipated variation voltage corresponds to maximum gain variations.

1       9. The circuit as claimed in claim 3, wherein said reference voltage source  
2 produces a sequence of two voltages with a difference corresponding to a  
3 predetermined voltage to enable said measurement circuit to determine an offset error  
4 in the correlated double sampling amplifier and/or A/D converter.

1       10. The circuit as claimed in claim 9, wherein said predetermined voltage  
2 corresponds to maximum offset variations.

1       11. The circuit as claimed in claim 3, wherein said reference voltage source  
2 produces a plurality of analog voltages ranging from analog ground to a full-scale  
3 voltage level to enable said measurement circuit to determine non-linearity errors in the  
4 A/D converter.

1           12. The circuit as claimed in claim 3, wherein said reference voltage source  
2 produces a voltage corresponding to a full-scale voltage level to enable said  
3 measurement circuit to determine a gain error in the correlated double sampling  
4 amplifier and/or A/D converter;  
5           said reference voltage source producing a voltage corresponding to ground to  
6 enable said measurement circuit to determine an offset error in the correlated double  
7 sampling amplifier and/or A/D converter; and  
8           said reference voltage source producing a plurality of analog voltages ranging  
9 from analog ground to a full-scale voltage level to enable said measurement circuit to  
10 determine non-linearity errors in the A/D converter.